RAB 2001-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: *Belgard, R.*	)	Art Unit: *unknown*
	)	
Serial No.: *unknown*	)	Examiner: *unknown*
	)	
Filed: *January 10, 2001*	)	
	)	
For: *Speculative Address Translation for Processor Using Segmentation and Optional Paging*	)	

PRELIMINARY AMENDMENT
FOR ACCOMPANYING RULE 1.60 CONTINUATION APPLICATION

Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

As part of the present filing, the Applicant respectfully submits the following to place this case in condition for allowance:

IN THE TITLE:

Please change the title to:

SPECULATIVE ADDRESS TRANSLATION FOR PROCESSOR USING SEGMENTATION AND OPTIONAL PAGING

IN THE SPECIFICATION:

Please insert the following sentences before line 1: "This application is a continuation of application serial no. 08/458,479 filed on June 2, 1995, now U.S. Patent No. 5,895,503 and a continuation of application serial no. 09/905,410 now U.S. Patent No. 5,960,466 filed August 4, 1997. The present application is also a continuation of serial no. 08/905,356 filed August 4, 1997.

IN THE CLAIMS:

Please cancel claims 1 - 37.

Please add new claims 38 - 66:

38. (New) A system for performing address translations in a processor employing both segmentation and optional independent paging the system comprising:

a page cache providing an actual physical page frame address from a virtual address in a time period T, the page frame cache accessed by using a page field of a fully calculated linear address; and

a speculative physical page frame address generator providing a speculative physical page address related to said virtual address in a time < T;

wherein the respective page frames are combined with offset portions to produce physical memory addresses.

39. (New) The system of claim 38, wherein the speculative physical page frame address can be used for generating a memory access faster than a memory access based on said actual physical page frame address.

40. (New) The system of claim 39 wherein the memory access is to a cache memory.

41. (New) The system of claim 39 including a cancellation circuit for canceling the memory access if the speculative physical page frame address and actual physical page frame address are different.

42. (New) The system of claim 38, wherein the speculative physical page frame address generator comprises a second page frame cache.

43. (New) The system of claim 38 wherein the speculative physical page frame address generator comprises a page frame address cache accessed during calculation of said fully calculated linear address.

44. (New) A circuit for performing memory accesses in a microprocessor system that uses a virtual address having a segment identifier and a segment offset, the circuit comprising:

a) a linear address generator adapted to calculate a calculated linear address based on processing the entire virtual address; and

b) a physical address generator, coupled to the linear address generator, adapted to generate a calculated physical address based on processing all of said calculated linear address, said physical address generator including a first memory for caching said calculated physical address; and

c) a second memory coupled to the linear address generator storing physical address information usable to generate a tentative physical address;

wherein said tentative physical address is used to initiate a tentative memory access that is completed unless said tentative physical address is different from said calculated physical address, in which case said calculated physical address is instead used for a calculated memory access.

45. (New) The circuit of claim 44, wherein said tentative physical address and said calculated physical address are generated in parallel, and said tentative physical address is completed before said calculated physical address can be completed by said physical address generator.

46. (New) The circuit of claim 45, wherein said tentative physical address is generated based on processing a portion of said calculated linear address.

47. (New) The circuit of claim 44, wherein said physical address information in said second memory is derived from a translation of a prior virtual address.

48. (New) The circuit of claim 44 wherein said first memory is a page cache located in a paging unit of the microprocessor.

49. (New) The circuit of claim 44, wherein said second memory includes segment descriptor information.

50. (New) The circuit of claim 46, wherein said calculated linear address is a 32 bit linear address, and said tentative physical address is based on a lower portion of said 32 bit linear address.

51. (New) The circuit of claim 44, wherein the tentative memory access and calculated memory access are to a cache memory.

52. (New) A computer system using segmentation and optional independent paging for performing address translations comprising:

an address translation memory capable of storing a portion of a physical address corresponding to a stored page frame;

a virtual to linear address converter circuit for generating a calculated linear address; and

a linear to physical address converter circuit for receiving and generating a calculated physical address based on the calculated linear address, the calculated physical address including a first page frame and a first page offset; and

a fast physical address circuit generating a fast physical address comprised of the stored page frame combined with a page offset portion derived from the virtual address;

wherein the fast physical address is generated prior to the generation of said calculated physical address.

53. (New) The system of claim 52, wherein the fast physical address can be used to initiate a fast memory access sooner than a memory access resulting from said first physical address.
54. (New) The system of claim 53, including a cancellation circuit for canceling the fast memory access if the fast physical address and first physical address are different.
55. (New) The circuit of claim 54, wherein the fast physical address is generated during the generation of the first linear address.
56. (New) The system of claim 55, wherein the stored page frame is generated in a prior address translation based on a prior virtual address.

57. (New) A method of generating a speculative memory address from a virtual address having both a segment identifier and a segment offset in a computer system employing both segmentation and optional independent paging, the method including the steps of:

(a) converting a portion of the virtual address into a partial linear address; and

(b) combining the partial linear address with physical address information obtained from a prior memory address generation to generate the speculative memory address.

58. (New) The method of claim 57, wherein the speculative memory address is used to initiate a speculative memory access.

59. (New) The method of claim 58 wherein the speculative memory access is to a cache memory.

60. (New) A method of performing memory references in a processor that employs both segmentation and optional independent paging during an address translation, said system comprising:

performing an actual address translation from a virtual address by first calculating a linear address based on both a segment identifier and an offset associated with the virtual address, and then generating an actual physical address based on the calculated linear address; and

performing a speculative address translation from the virtual address using portions of the linear address and actual physical address information from a prior virtual address translation to produce a speculative physical address;

performing a memory reference using the speculative physical address;

validating that the memory reference is valid.

61. (New) The method of claim 60 wherein the validating step comprises comparing the page frame portions of the actual physical address and the speculative physical address.

62. (New) The method of claim 61, further including a step of canceling the memory reference if the page frame portions of the actual physical address and the speculative physical address are different.

63. (New) A method of performing memory accesses in a microprocessor system using a virtual address having a segment identifier and a segment offset, the method comprising the steps of:
    (a) generating a calculated linear address based on processing said entire virtual address;
    (b) using a first cache containing physical address information to generate a calculated physical address based on said calculated linear address;
    (c) using a second cache containing physical address information to generate a tentative physical address in parallel with step (a) and before step (b) is completed, said tentative physical address being based in part on a portion of said calculated linear address;
    (d) using said tentative physical address to initiate a tentative memory access to a cache;
    (e) completing said tentative memory access to said cache when said tentative physical address and said calculated physical address are the same;
    (f) aborting said tentative memory access and performing a second memory access based on said calculated physical address when said tentative physical address and said calculated physical address are different.
64. (New) The method of claim 63, wherein said first cache is a page cache located in a paging unit of the microprocessor.
65. (New) The method of claim 63, wherein said second cache includes segment descriptor information.
66. (New) The method of claim 63, wherein said calculated linear address is a 32 bit linear address, and said tentative physical address is based on a lower portion of said 32 bit linear address.

Remarks

Original claims 1 - 36 have been canceled. Claims 38 - 66 are presently pending.

The present claims are believed to be in patentable form as they recite structures and methods not disclosed or suggested in the art.

Should the Examiner believe it is necessary or fruitful to discuss any of the above points in person, Applicant is open to a teleconference (415-551-8298) at any convenient time.

Respectfully submitted,

Law+

Date: January 10, 2001

J. Nicholas Gross, Attorney, Reg. No. 34,175

I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner of Patents and Trademarks, this 10th of January 2001.